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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,305	02/28/2002	Stephen M. Trimberger	X-874 US	7532

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,305	TRIMBERGER, STEPHEN M.	
	Examiner	Art Unit	
	James C Kerveros	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/28/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-39 are pending and are hereby presented for examination, in response to the present Application filed 2/28/2002.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the feature of "data communications link" recited in Claims 2, 10, 21, 26, 34, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-9, 11, 12, 14, 16-19, 25, 27- 29, 31-33, 35, 36, 38 and 39 are rejected under 35 U.S.C. 102(b) as being anticipated by McClintock et al. (US 6166559).

Regarding independent Claims 1, 25, McClintock discloses a method for redundant circuitry for a programmable logic device (PLD) for repairing the (PLD) by replacing a defective logic area with a redundant logic circuit, comprising:

Testing a programmable logic device (36, FIG. 2) during the manufacturing process and selecting a plurality of defective logic areas (38) containing localized defects. If it is determined that one of logic areas 38 is defective, then the manufacturer provides redundancy configuration data to programmable logic device 36 at input 64 that identifies which logic area 38 is defective. The redundancy configuration data is used by programmable logic device 36 to redirect programming data into a redundant logic area (i.e., the center logic area 38) instead of the defective logic area.

Recording defect data (150, FIG. 3) for each defective logic areas 38, including identifier and location information corresponding to a defective logic area. If a defect 150 is detected in logic area No. 9, then redundant logic area No. 5 can be used to replace logic area No. 9. Once the defect has been located, redundancy configuration data identifying the location of the defect is stored by the manufacturer in redundancy configuration data storage 66 and maintaining a database of the defect data corresponding to the defective logic areas (FIG. 2).

Receiving from a user a location identifier with the programming data, which is provided by a user to programmable logic device 36 at input 70. Programming data is used to configure the identified location of programmable logic area 38, FIG. 2.

Providing to the user location information from the database (66) corresponding to defect data (150, FIG. 3) for each defective logic areas 38, including identifier and location information.

Regarding independent Claims 9, 33, McClintock discloses the pertinent limitations as applied to claim 1 above, and in addition he discloses creating and

implementing a user design in the programmable logic device 106 of FIG. 3. A programmable logic device programmer (not shown in FIG. 3) is used to supply the programming data to input 108, which specifies the logic design to be implemented on programmable logic device 106.

Also, programming data stored in (208) which is applied to associated logic regions 212 to implement the logic design desired by the user. If a defect is detected in, for example, the right column of logic regions 212 in FIG. 8, then multiplexers 210 are configured by the manufacturer to redirect programming data to output lines 214, thus shifting the programming data from the left multiplexer 210 into programming data storage 216 in the redundant column where it is applied to redundant logic regions 218.

Regarding Claims 3, 4, 11, 12, McClintock discloses location information on defective PLDS including identification information for defective logic areas 38 and wherein the location information specifies the location of each localized defect, 38, FIGS. 2 and 3.

Regarding Claim 5, 27, McClintock discloses implementing a user design with a programmable logic device programmer (not shown in FIG. 3), which is used to supply the programming data to input 108, which specifies the logic design to be implemented on programmable logic device 106.

Regarding Claim 6, 28, 35, with respect to claimed limitation of "receiving a second identifier from a user and providing to the user location information from the database corresponding to the second identifier", McClintock discloses a first identifier corresponding to a second defective logic area, which is similar to the second identifier

corresponding to a second defective logic area (38, FIGS. 2 and 3. As, described previously, McClintock discloses the steps of receiving from a user a location identifier with the programming data, which is provided by a user to programmable logic device 36 at input 70. Programming data is used to configure the identified location of programmable logic area 38, FIG. 2 and further providing to the user location information from the database (66) corresponding to defect data (150, FIG. 3) for each defective logic areas 38, including identifier and location information.

Regarding Claim 7, 16, 23, 29, 36, McClintock discloses a programmable logic device (PLD) which is a commonly used in as a field programmable gate array (FPGA).

Regarding Claim 8, 17-19, 24, 30-32, 38, 39, McClintock discloses a process of repairing a logic device that contains defective circuitry, which involves remapping the logic of the redundant logic area (i.e., the normally unused logic area on a defect-free device) into the defective logic area by redirecting the programming data that would normally have been directed into the defective logic area into the redundant logic area and by redirecting the programming data that would normally have been used by the redundant logic area to ensure that the redundant logic area is inactive or unused on a defect-free device into the defective logic area, using data path remapping circuitry 80, FIGS. 1-3.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

> to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 10, 13, 15, 20-24, 26, 30, 34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClintock et al. (US 6166559).

Regarding Claims 20, 13, 15, 22, McClintock substantially discloses the pertinent claimed invention as applied to claims 1 and 9, above. However, McClintock does not explicitly disclose performing an incremental compilation with respect to a first design file, then generating a second design file and providing the second design file to the user. However, as described above, McClintock discloses creating and implementing a user first design in the programmable logic device 106 of FIG. 3, where a programmable logic device programmer (not shown in FIG. 3) is used to supply the programming data to input 108, which specifies the logic design to be implemented on programmable logic device 106. Furthermore, it is well known in the art to perform an incremental compilation with respect to a file. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use program compilation techniques in the method of McClintock, which are well known in the art, for the purpose of generating a second design file. A person skilled in the art would have been motivated to use a well-known cost effective programming compiler so as to avoid extra development cost and time associated with new program development.

Regarding Claims 2, 10, 21, 26, 34, McClintock does not explicitly disclose a data communications link for receiving the first identifier from the user and providing to the user location information from the database. However, McClintock discloses

receiving location identifier related to defective logic areas and providing to the user location information from the database corresponding to defect data (150, FIG. 3). Furthermore, it is well known in the art to transmit and receive data over a communications link through a computer network such as the Internet. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a well known Internet communications link between a programmable logic device (PLD) and a user, in the method of McClintock, so the user may have remote access to repair data associated with defective programmable logic devices (PLDS).

Regarding Claims 30, 37, McClintock does not explicitly disclose device-specific information relating to the speed of various sub-components of the PLD. However, it is well known in the art, the speed information is normally furnished in a data sheet by the manufacturer for a particular component, which also varies per manufacturer. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to obtain speed information for a PLD, using the data sheet supplied by the manufacturer, in the method of McClintock, thus avoiding elaborate speed calculation.

Conclusion

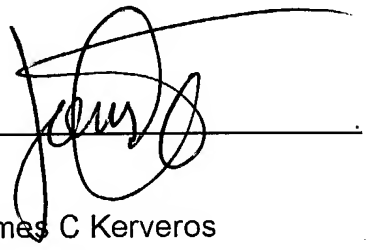
Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 3 September 2004
Office Action: Non-Final Rejection

By: 

James C Kerveros
Examiner
Art Unit 2133

GUY J. LAMARRE
PRIMARY EXAMINER